Cal Poly Pomona

Two 3x8 Decoders to 4x16 Decoder to 7-Segment Display

Experiment 5

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9/25/2025

0.0 PRELAB

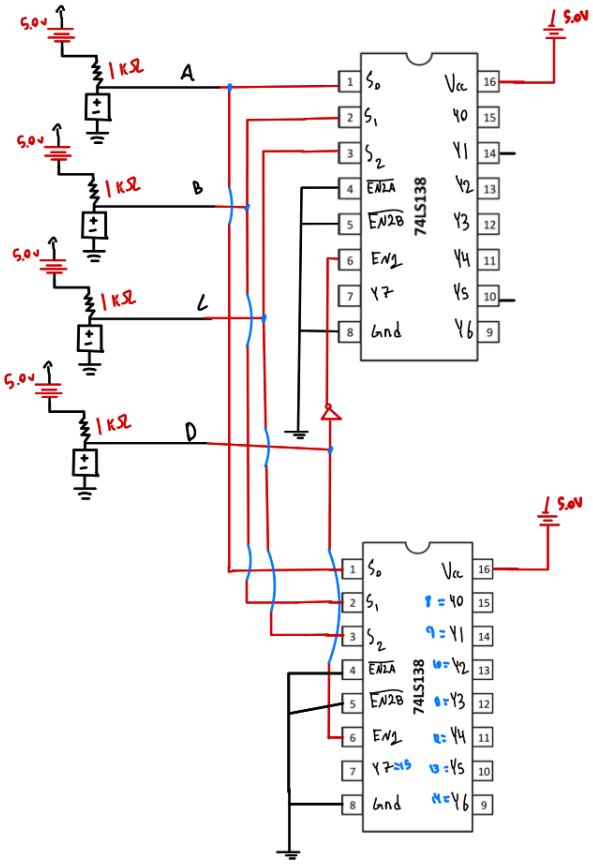
0.1 Design a 4x16 decoder using a minimum number of 74138 and logic gates.

We will be using the enable switch of the two 3x8 decoders to act as a 4th input D, inverting the signal initially as the 74138 chip is enabled low. This is shown in Table 0.1 & in Figure 0.1 below.

Table 0.1 : Two 3x8 -> 4x16 Decoder Circuit Truth Table

E1 (D)	C	B	A	Maxterm
0	0	0	0	M0
0	0	0	1	M1
0	0	1	0	M2
0	0	1	1	M3
0	1	0	0	M4
0	1	0	1	M5
0	1	1	0	M6
0	1	1	1	M7
1	0	0	0	M8
1	0	0	1	M9
1	0	1	0	M10
1	0	1	1	M11
1	1	0	0	M12
1	1	0	1	M13
1	1	1	0	M14
1	1	1	1	M15

Figure 0.1 : Two 3x8 -> 4x16 Decoder Circuit Schematic



0.2 Design a logic using a minimum of 74138s (3 x 8 decoders) to generate the minterms m1 , m5 and m9 based on the four switch inputs S3, S2,S1, S0. Then display the selected minterm numbers (1 or 5 or 9) on a seven segment display by generating a 4-bit input (W,X,Y,Z) for a BCD to seven-segment code converter. Turn an LED ON for all other minterms and blank the seven-segment display. Note that these four inputs (W,X,Y,Z) can be obtained from the selected output line (1 or 5 or 9) of the decoders that is generated by the four input switches (S3, S2, S1, S0). Use a minimum number of logic gates. Determine the truth table, and then draw a logic diagram.

Table 0.2 : WXYZ Truth Table

MinTerm	W	X	Y	Z
m1	0	0	0	1
m5	0	1	0	1
m9	1	0	0	1
Theoretical Inputs:	m9	m5	Gnd	Vcc
Actual Inputs	(M9)’	(M5)’	Gnd	Vcc

NOTE: In order to get minterms for 74138s, we have inverted the outputs because 74138s are maxterms generators.

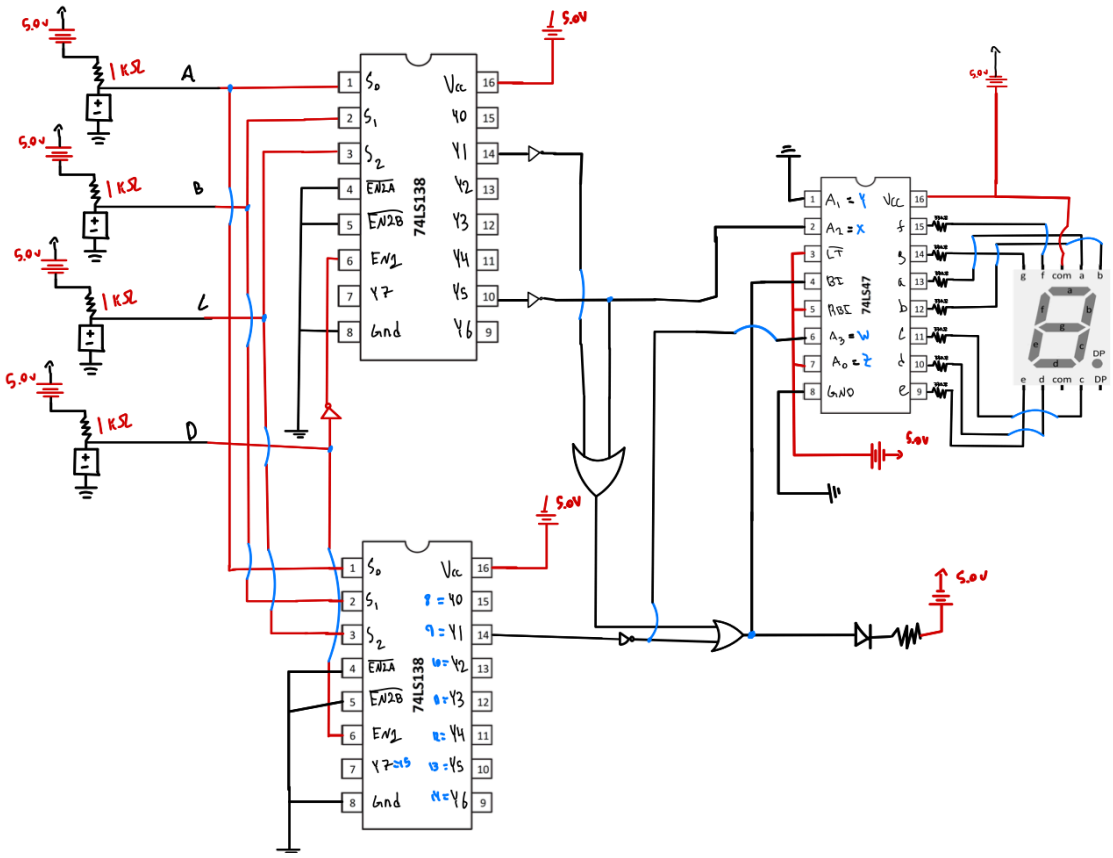
Combinational Logic Derivation

Below we show the derivation for the combinational circuit we derived to shut off the display (which is enable HIGH), and turn on the LED for every input besides those that generate minterms m1, m5, & m9.

m1+m5+m9 = 1	Theoretical
(M1)’+(M5)’+(M9)’ = 1	Actual

Resulting output will split partially into to the Blanking Input for the 74SL47 chip, that will go LOW and shut off the display whenever it isn’t m1, m5, & m9. The other split will go to a LED connected to Vcc, so whenever it is enable LOW, the LED will be on. This is shown below in figure 0.2.

Figure 0.2 : Combinational Circuit Schematic



1.0 **INTRODUCTION**

Implement the above circuit from the pre-lab using a minimum number of decoder and gates. Demonstrate the operations using switches and LED, Seven segments display etc. as needed. Schematics will be pulled from Pre-Lab when needed.

2.0 **OBJECTIVES**

The goal is the following:

1. Generate minterms m1, m5, m9 from the decoder outputs.
2. Encode these minterms to BCD (W,X,Y,Z) and drive a 7-segment via 74LS47 (display 1/5/9).
3. Blank the display and light an “OTHER” LED for all non-selected minterms.
4. Verify operation across all 16 input combinations.

3.0 **REQUIREMENT**

Implement the 4×16 decoder and the m1/m5/m9 selector/encoder so that inputs S3..S0 produce: 1, 5, or 9 on the seven-segment when S3S2S1S0 = 0001, 0101, 1001 respectively; otherwise the seven-segment is blank and the OTHER LED is ON.

Table 1.1 - Truth Table of Combinational Circuit

MinTerm	S3	S2	S1	S0	7-Seg	LED
m1	0	0	0	1	1	Off
m5	0	1	0	1	5	Off
m9	1	0	0	1	9	Off
All others	All others	All others	All others	All others	blank	On

4.0 **PARTS LIST**

The Parts list for this experiment is shown below in Table 4.1

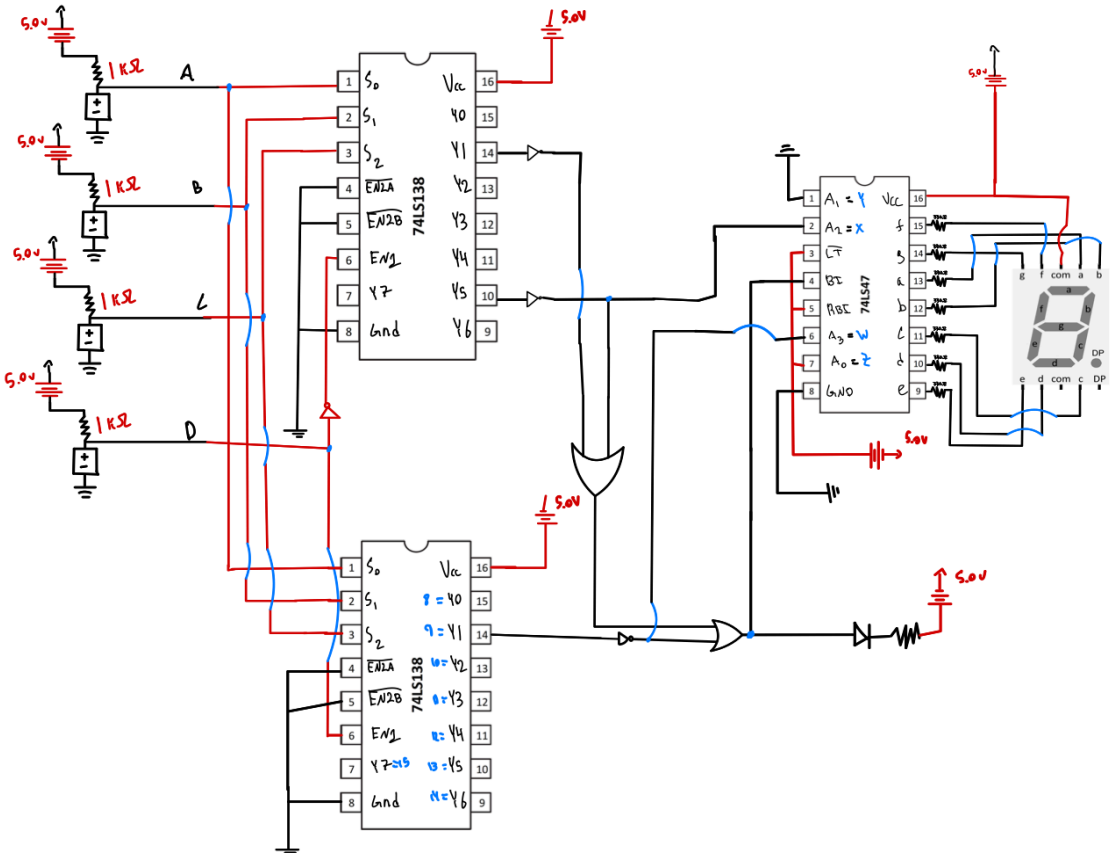
Table 4.1 - Parts List

Item No.	Part Number	Function	Quantity
1	74LS138	3-to-8 Decoder	2
2	74LS04	Inverter	1
3	74LS32	OR	1
4	74LS47	BCD-to-7-Seg	1
5	7-Segment	Output	1
6	DIP Switch	Input	1
7	LED	Output	1

5.0 **DESIGN/IMPLEMENTATION**

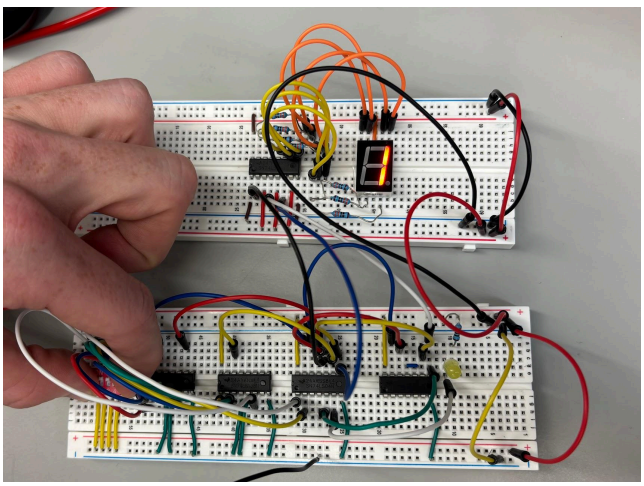
The design from figure 0.2 in the prelab will be tested, and it will be shown again below in figure 5.1. A dip switch will be used to provide the inputs to the 3-to-8 decoders, and the outputs will be displayed using a 7-segment display and LED.

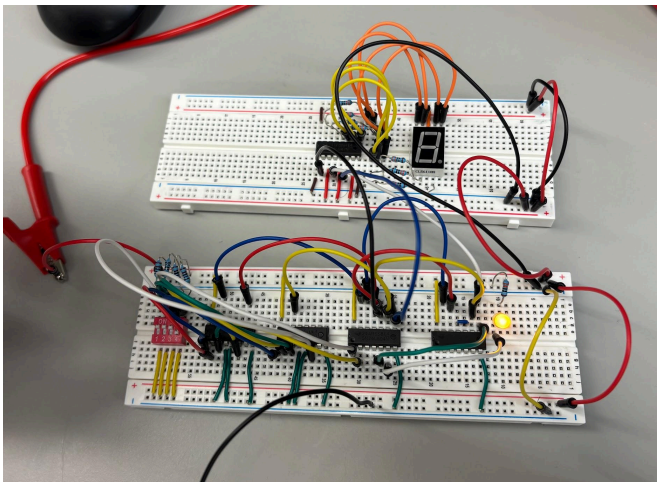
Figure 5.1



6.0 **TEST SETUP**

Below is an image of the breadboard The DIP switches provide S3..S0. Two 74LS138s implement the 4×16 decoder as described. The selected minterm (m1/m5/m9) is encoded to BCD and shown on the 7-segment via the 74LS47. For all other inputs, the display is blanked and the OTHER LED lights. The breadboard photo below shows both the decoder and the display/LED interface.





7.0 **TEST RESULTS/VERIFICATION MATRIX**
The test results are summarized below in Table 7.1:

Table 7.1 - Truth Table of Circuit

S3	S2	S1	S0	Selected Minterm	W	X	Y	Z	7-Seg	LED
0	0	0	0	m0	-	-	-	-	blank	On
0	0	0	1	m1	1	0	0	0	1	Off
0	0	1	0	m2	-	-	-	-	blank	On
0	0	1	1	m3	-	-	-	-	blank	On
0	1	0	0	m4	-	-	-	-	blank	On
0	1	0	1	m5	1	0	1	0	5	Off
0	1	1	0	m6	-	-	-	-	blank	On
0	1	1	1	m7	-	-	-	-	blank	On
1	0	0	0	m8	-	-	-	-	blank	On
1	0	0	1	m9	1	0	0	1	9	Off
1	0	1	0	m10	-	-	-	-	blank	On
1	0	1	1	m11	-	-	-	-	blank	On
1	1	0	0	m12	-	-	-	-	blank	On
1	1	0	1	m13	-	-	-	-	blank	On
1	1	1	0	m14	-	-	-	-	blank	On
1	1	1	1	m15	-	-	-	-	blank	On

8.0 Conclusion
The 4×16 decoder constructed from two 74LS138s operated correctly, activating exactly one active-low minterm per input code. Using m1, m5, and m9, we generated BCD inputs (W,X,Y,Z) to the 74LS47 and the 7-segment displayed the digits 1, 5, and 9. For all other inputs, the

display was blanked and the other indicator LED lit up. The measurements across all 16 input combinations matched the expected behavior in Table 7.1.

9.0 Post Lab

Design a combinational circuit to generate the following:

F0 = SUM (m(1,3,4))

F1 = SUM (m(0,2,4,7))

F2 = SUM (m(0,1,3,5,6))

F3 =SUM (m(2,6))

Draw a logic diagram using a 74138 decoder and external gates.